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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/017,047 | 12/13/2001 | Matthew A. Hayduk | 42390P12401 | 6573 |

8791 7590 02/27/2004

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| EXAMINER | |
|---|---|
| ALI, SYED J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2127 | 3 |

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/017,047 | HAYDUK, MATTHEW A. | |
| | Examiner | Art Unit | |
| | Syed J Ali | 2127 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. Claims 1-27 are pending in this application.

### *Claim Objections*

2. Claims 6 and 25-27 are objected to because of the following informalities:

In claim 6, line 1, "wherein the wherein the first monitor..." should read "wherein the first monitor..."

In claims 25-27, line 2, "result:" should read "results in:"

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 6-7, 10, 15-16, 18, 22-25, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Hardwick (USPN 6,292,822).

5. As per claim 1, Hardwick teaches the invention as claimed, including an apparatus comprising:

a first processor to execute a first set of instructions (col. 7 lines 49-65, "This distributed memory architecture includes a number of processors 20, 22, 24, each with a corresponding memory 26, 28, 30. The processors execute code and operate on data stored in their respective memories");

a second processor to execute a second set of instructions (col. 7 lines 49-65, "This distributed memory architecture includes a number of processors 20, 22, 24, each with a corresponding memory 26, 28, 30. The processors execute code and operate on data stored in their respective memories");

a first monitor adapted to determine available performance capability of the first processor while executing the first set of instructions (col. 4 lines 24-40, "The dynamic load balancing method distributes processing workload by evaluating the computational cost of a function call at runtime and determining whether or not to ship the call to another processor"); and

a second monitor communicatively coupled to the first monitor and adapted to determine available performance capability of the second processor while executing the second set of instructions, wherein the apparatus is adapted to execute a third set of instructions on the first processor when the available performance capability of the second processor is less than an acceptable performance level to execute the third set of instructions (col. 4 lines 24-40, "Before invoking a function call, a processor of the parallel computer determines whether the computational cost of the function call exceeds a threshold. If so, it determines whether another processor is available to process the function call. If another processor is available, the processor seeking help ships the arguments of the call to the available processor and receives the results").

6. As per claim 2, Hardwick teaches the invention as claimed, including the apparatus of claim 1, further comprising memory to store the first, second, and third set of instructions (col. 7 lines 49-65, "This distributed memory architecture includes a number of processors 20, 22, 24, each with a corresponding memory 26, 28, 30. The processors execute code and operate on data stored in their respective memories").

7. As per claim 6, Hardwick teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is provided, at least in part, by a fourth set of instructions being executed on the first processor (col. 5 lines 1-15, "When processing proceeds to a point where a processor can seek help from another processor, the processor executes the test function and evaluates the computational cost").

8. As per claim 7, Hardwick teaches the invention as claimed, including the apparatus of claim 6, wherein the first monitor is provided in part by logic circuitry within the first processor (col. 5 lines 1-15, "When processing proceeds to a point where a processor can seek help from another processor, the processor executes the test function and evaluates the computational cost", wherein the processor is implemented in logic gates, and the functionality of the monitor is executed within the processor).

9. As per claim 10, Hardwick teaches the invention as claimed, including the apparatus of claim 1, wherein the acceptable performance level is defined by a user (col. 37 lines 22-35, "The

threshold therefore acts as a tuning function for the load-balancing system. Since it is dependent on many factors, including the algorithm, architecture, MPI implementation, problem size, machine size, and input data, it can be supplied as either a compile-time or run-time parameter", wherein the parameters are supplied by the user with respect to the particular system needs).

10. As per claim 15, Hardwick teaches the invention as claimed, including a method comprising:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions (col. 6 lines 14-21, "When the manager receives a request for help [706], it checks the list for idle processors").

11. As per claim 16, Hardwick teaches the invention as claimed, including the method of claim 15, further comprising determining an available capacity of the second processor while the second processor is executing a second set of instructions (col. 35 lines 48-62, "The preprocessor inserts a load-balance test function into the sequential version of every divide-and-conquer function. This test determines whether to ask the manager for help with one or more of the recursive function calls", wherein the determination is based on the processor's capacity to process additional function calls).

12. As per claim 18, Hardwick teaches the invention as claimed, including the method of claim 15, further comprising determining if the capacity of the first processor is sufficient to

execute the first set of instructions within a user defined performance level (col. 36 lines 23-35, "In its message loop, the idle processor blocks waiting for a message. On receiving the message from the manager [806], it sets up appropriate receive buffers for the argument [808], and then sends the requesting processor an acknowledgement message signaling its readiness").

13. As per claim 22, Hardwick teaches the invention as claimed, including the method of claim 15, further comprising reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions (col. 36 lines 36-54, "The idle processor receives the function arguments via a reply message [812] to its acknowledge message from the requesting processor. In response to this message, the idle processor invokes the function on the function's arguments [814], and sends the results back to the requesting processor [816]. It then notifies the manager that it is once again idle [818], and waits for another message by returning to its message loop", wherein a processor going into idle mode reduces its power consumption since it is not performing any processing).

14. As per claim 23, Hardwick teaches the invention as claimed, including the method of claim 22, further comprising reducing the voltage potential of the first processor (col. 36 lines 36-54, wherein a processor going into idle mode reduces its power consumption since it is not performing any processing, and the reduction in power therein inherently reduces the voltage potential of the processor).

15. As per claim 24, Hardwick teaches the invention as claimed, including an article of manufacture comprising a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions (col. 6 lines 14-21, "When the manager receives a request for help [706], it checks the list for idle processors").

16. As per claim 25, Hardwick teaches the invention as claimed, including the article of claim 24, wherein the instructions, when executed, further results in:

determining if the capacity of the first processor is sufficient to execute the first set of instructions within a user defined performance level (col. 36 lines 23-35, "In its message loop, the idle processor blocks waiting for a message. On receiving the message from the manager [806], it sets up appropriate receive buffers for the argument [808], and then sends the requesting processor an acknowledgement message signaling its readiness").

17. As per claim 27, Hardwick teaches the invention as claimed, including the article of claim 24, wherein the instructions, when executed, further results in:

reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions (col. 36 lines 36-54, "The idle processor receives the function arguments via a reply message [812] to its acknowledge message from the requesting processor. In response to this message, the idle processor invokes the function on the function's

arguments [814], and sends the results back to the requesting processor [816]. It then notifies the manager that it is once again idle [818], and waits for another message by returning to its message loop", wherein a processor going into idle mode reduces its power consumption since it is not performing any processing).

### *Claim Rejections - 35 USC § 103*

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick in view of Dean et al. (USPN 6,317,840) (hereinafter Dean).

20. As per claim 3, Dean teaches the invention as claimed, including the following limitations not shown by Hardwick, specifically the apparatus of claim 2, wherein the set of instructions comprise instructions of a program selected from the group consisting of an application program and an operating system program (col. 3 lines 44-67, "Pursuant to traditional processor operations, processor instructions are loaded into pipeline 12 and subsequently dispatched for execution", wherein the instructions fetched from memory may be related to any sort of software the system runs).

It would have been obvious to one of ordinary skill in the art to combine Hardwick with Dean since the method of load balancing disclosed by Hardwick is limited to processing of parallel programs. Specifically, parallel programs are converted to sequential code, and function calls are evaluated before they are either executed or shipped to another processor. Dean, while providing a system that implements multiple functional units within a single processor, would provide a means of determining which of multiple processors is best suited to process any instruction. Specifically, Hardwick teaches the invention as claimed, including the use of a manager to control the load balancing, which is similar in functionality to the control mechanism in Dean. To determine which processor is best suited to process an instruction, as in Dean, would have been an obvious modification to Hardwick, since it would allow the load balancing mechanism to be applied to any instruction, instead of being limited to parallel programs that had been converted to a sequential algorithm.

21. As per claim 4, Dean teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is adapted to determine the available performance capacity based on a current operational voltage potential of the first processor (col. 1 line 55 - col. 2 line 12, "It is recognized that power consumption is directly related to the amount of toggling of wires or nets within a circuit. Each time a wire toggles between a low and high voltage level, a certain amount of power is consumed").

22. As per claim 5, Dean teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is adapted to determine the available performance capacity based on

an operational frequency of the first processor (col. 1 line 55 - col. 2 line 17, "a solution for power reduction is needed even after the clock has been slowed to its lowest frequency. Without a processor that can deliver low power performance, battery powered applications cannot be fully exploited").

23. Claims 8-9, 19, 21, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick in view of Chen et al. (US 2003/0012143) (hereinafter Chen) in view of Blank et al. (USPN 6,496,823) (hereinafter Blank).

24. As per claim 8, Blank teaches the invention as claimed, including the following limitations not shown by Hardwick, specifically using information about a system to perform predictive load balancing of work to be processed (col. 5 lines 12-27, "The apportioning system 124 of the present invention apportions a work unit across multiple processors to give faster processors more work than slower processor s that all the processors complete in approximately the same amount of time. The apportioning system 124 achieves this by taking into account system configuration factors that have a substantial impact on the optimization of an allocation").

Chen teaches the invention as claimed, including the following limitations not shown by Hardwick or Blank, specifically the information about the system is maintained in a database to track an historical average of a processor demand needed for a user (paragraph 0009, "Network resource manager 110 includes a demand history database 112, a demand prediction processor 114, a cost function database 116, a resource pool 118, a decision history database 120 and a network resource allocator 122").

It would have been obvious to one of ordinary skill in the art to combine Hardwick, Blank, and Chen since the load balancing mechanism of Hardwick only reallocates tasks to be processed on a dynamic basis. Specifically, a function call is submitted to a processor, which then determines if the processor has a sufficient capability to process the task. If so, the processor executes the task, and if not, it requests the manager to redistribute the task to another processor. If a determination can be made that another processor is better suited to execute the function call before the task is distributed to a processor, costly overhead of shipping the call to another processor can be avoided. Thus, the method of Blank provides such a mechanism, by determining the available processing capacity, in terms of MIPS, of each processor in the system, as well as taking into account the processing speed of the processor. Thus, an initial load balancing can be performed, possibly avoiding shipping function calls based on an initial processing power value of the processor. However, the method of predictive load balancing exhibited in Blank fails to take into account variations in demand from task to task. Rather, an assumption is made that each task to be processed puts the same workload upon the processor. Thus, a historical database for keeping track of past performance, as in Chen, would have been an obvious modification to Hardwick and Blank. Although Chen uses the historical database to monitor past performance based on users of a system rather than tasks, the predictive model is applicable to tasks as well, and can be used for dynamic allocation and reallocation of tasks among processors, in accordance with the methods of Hardwick and Blank.

25. As per claim 9, Blank teaches the invention as claimed, including the apparatus of claim 8, wherein the database includes an average million instructions per second [MIPS] to execute

the third set of instructions (col. 6 lines 44-50, "Different measures may be used to determine the processing power value. For example, a rating for the number of million of instructions per second [MIPS] the processor is capable of executing may be used as a processor power value").

26. As per claim 19, Blank teaches the invention as claimed, including the method of claim 18, further comprising using information about a system to perform predictive load balancing of work to be processed (col. 5 lines 12-27, "The apportioning system 124 of the present invention apportions a work unit across multiple processors to give faster processors more work than slower processor s that all the processors complete in approximately the same amount of time. The apportioning system 124 achieves this by taking into account system configuration factors that have a substantial impact on the optimization of an allocation").

Chen teaches the invention as claimed, including the following limitations not shown by Hardwick or Blank, specifically the information about the system is maintained in a database to track an historical average of a processor demand needed for a user (paragraph 0009, "Network resource manager 110 includes a demand history database 112, a demand prediction processor 114, a cost function database 116, a resource pool 118, a decision history database 120 and a network resource allocator 122").

27. As per claim 21, Blank teaches the invention as claimed, including the method of claim 19, further comprising storing the historical average execution requirements in a table (col. 5 line 62 - col. 6 line 5, "Relational databases are organized into tables which consist of rows and columns of data", wherein a relational database is the model used by Blank).

28. As per claim 26, Blank teaches the invention as claimed, including the article of claim 25, wherein the instructions, when executed, further results in:

using information about a system to perform predictive load balancing of work to be processed (col. 5 lines 12-27, "The apportioning system 124 of the present invention apportions a work unit across multiple processors to give faster processors more work than slower processor s that all the processors complete in approximately the same amount of time. The apportioning system 124 achieves this by taking into account system configuration factors that have a substantial impact on the optimization of an allocation").

Chen teaches the invention as claimed, including the following limitations not shown by Hardwick or Blank, specifically the information about the system is maintained in a database to track an historical average of a processor demand needed for a user (paragraph 0009, "Network resource manager 110 includes a demand history database 112, a demand prediction processor 114, a cost function database 116, a resource pool 118, a decision history database 120 and a network resource allocator 122").

29. Claims 11-14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick in view of Conary et al. (USPN 5,842,029) (hereinafter Conary).

30. As per claim 11, Conary teaches the invention as claimed, including the following limitations not shown by Hardwick, specifically the apparatus of claim 1, wherein the apparatus is adapted to increase the available performance capability of the second processor when the

available performance capability of the first processor is less than the acceptable performance level to execute the third set of instructions on the first processor (col. 6 lines 9-32, "the core clock signals are referred to as phase one [PH1] and phase two [PH2]. The present invention also generates clock signals which are referred to as power up phase one [PUPH1] and power up phase two [PUPH2]. The PUPH1 and PUPH2 clock signals are the same as the PH1 and PH2 clock signals and clock the operation of control logic responsible for placing the processor in an out of a reduced power consumption state", wherein the processor powers up when the performance of the processor is sought to be increased).

It would have been obvious to one of ordinary skill in the art to combine Hardwick with Conary since in cases where the load balancing mechanism of Hardwick determines that no additional processors are available to offload extra work from a heavily loaded processor, an alternative method of servicing the processing is available. That is, if no processors can alleviate the processing load, the processor requesting assistance could utilize the method of Conary to increase the number of available processing cycles, thereby improving the performance of the processor. Furthermore, Conary provides the added benefit of allowing processors to go into a reduced power mode during periods of inactivity. This adds an extra dimension of efficiency to the overall system, while also implementing a dynamic load balancing technique.

31. As per claim 12, Conary inherently teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase the MIPS available on the first processor (col. 6 lines 9-32, wherein increasing the processing capabilities of a processor

increases the number of clock cycles, thereby increasing the number of MIPS available on the processor).

32. As per claim 13, Conary teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase an operational voltage potential of the first processor (col. 15 lines 17-26, "The control voltage drives the output of VCO 905. As the control voltage increases, the frequency output by the VCO 905 gets higher", wherein an increase in the voltage potential of the processor also increases the operational frequency of the processor, thereby generating additional processing cycles in the same elapsed time period).

33. As per claim 14, Conary teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase an operational frequency of the first processor (col. 15 lines 17-26, "The control voltage drives the output of VCO 905. As the control voltage increases, the frequency output by the VCO 905 gets higher", wherein an increase in the voltage potential of the processor also increases the operational frequency of the processor, thereby generating additional processing cycles in the same elapsed time period).

34. As per claim 20, Conary teaches the invention as claimed, including the method of claim 18, further comprising increasing the available capacity of the second processor if the capacity of the first processor is not sufficient to execute the first set of instructions within the user defined performance level (col. 6 lines 9-32, "the core clock signals are referred to as phase one [PH1] and phase two [PH2]. The present invention also generates clock signals which are referred to as

power up phase one [PUPH1] and power up phase two [PUPH2]. The PUPH1 and PUPH2 clock signals are the same as the PH1 and PH2 clock signals and clock the operation of control logic responsible for placing the processor in an out of a reduced power consumption state", wherein the processor powers up when the performance of the processor is sought to be increased).

35. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick in view of Blank.

36. As per claim 17, Blank teaches the invention as claimed, including the method of claim 16, wherein determining the available capacity of the second processor includes determining an available million instructions per second [MIPS] of the second processor (col. 6 lines 44-50, "Different measures may be used to determine the processing power value. For example, a rating for the number of million of instructions per second [MIPS] the processor is capable of executing may be used as a processor power value").

It would have been obvious to one of ordinary skill in the art to combine Hardwick with Blank since the load balancing mechanism of Hardwick only reallocates tasks to be processed on a dynamic basis. Specifically, a function call is submitted to a processor, which then determines if the processor has a sufficient capability to process the task. If so, the processor executes the task, and if not, it requests the manager to redistribute the task to another processor. If a determination can be made that another processor is better suited to execute the function call before the task is distributed to a processor, costly overhead of shipping the call to another processor can be avoided. Thus, the method of Blank provides such a mechanism, by

determining the available processing capacity, in terms of MIPS, of each processor in the system, as well as taking into account the processing speed of the processor. Thus, an initial load balancing can be performed, possibly avoiding shipping function calls based on an initial processing power value of the processor.

***Conclusion***

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

USPN 4,270,167 to Koehler et al. discloses monitoring the status of an executing processor.

USPN 4,495,570 to Kitajima et al. discloses distributing processing requests among a plurality of processors based on current status of the processors.

USPN 6,570,571 to Morozumi discloses distributing processing requests among a plurality of processors based on load information generated internally to a processor and broadcasted to the system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Syed Ali
February 9, 2004

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